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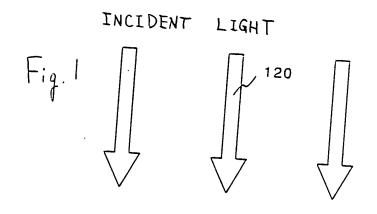
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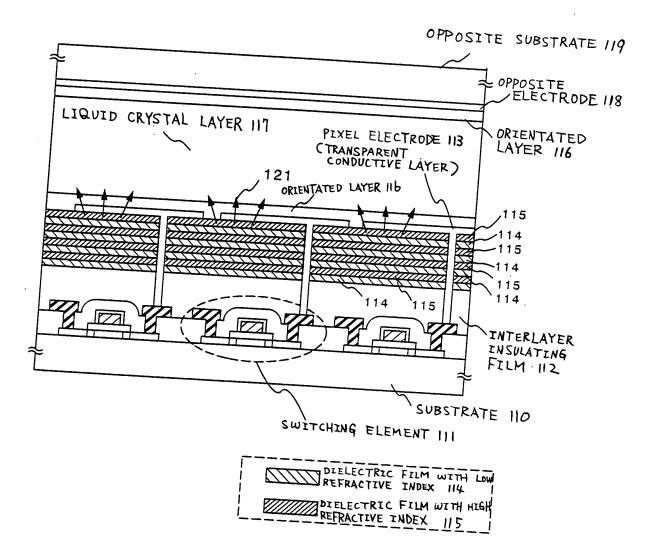
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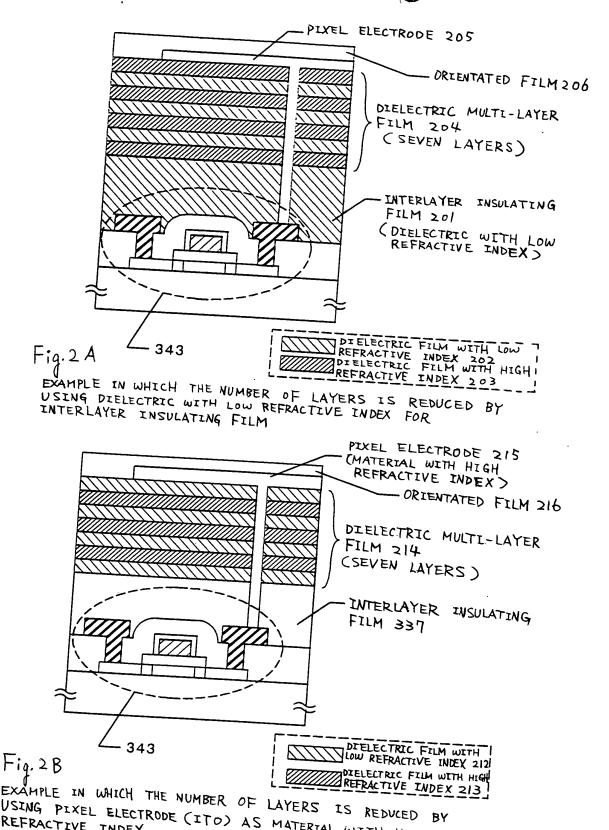
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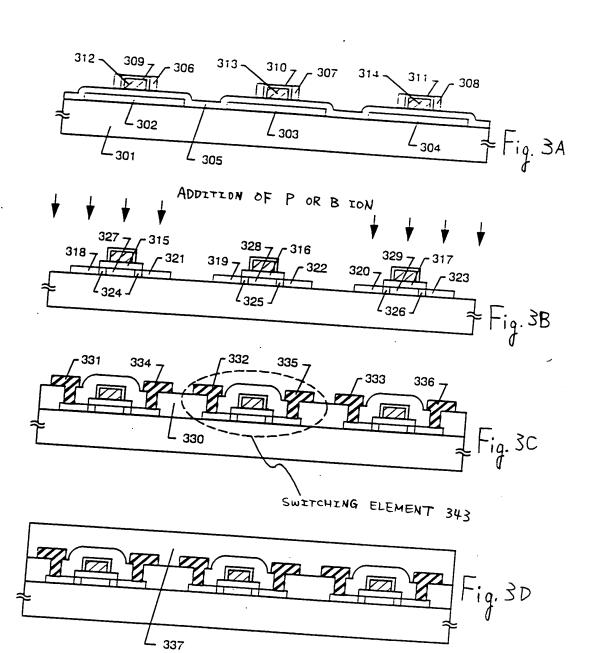


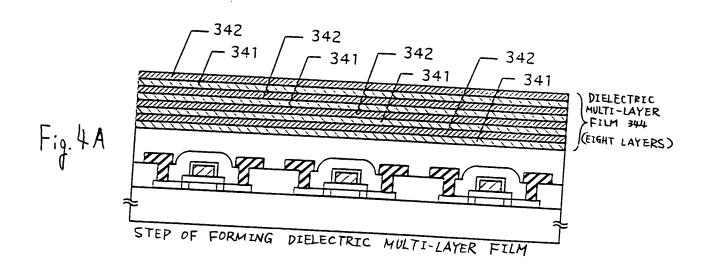


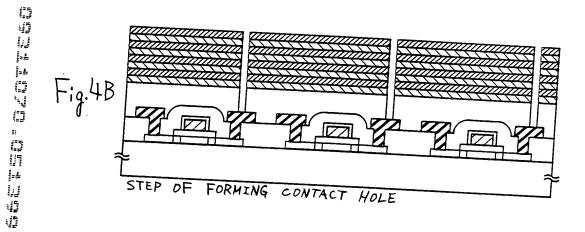
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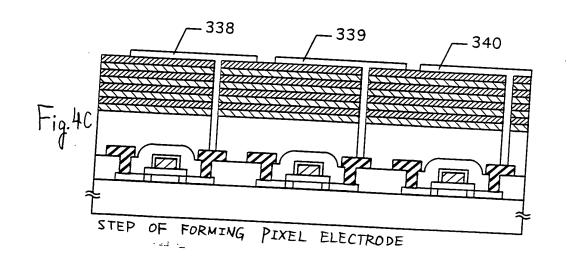


EXAMPLE IN WHICH THE NUMBER OF LAYERS IS REDUCED BY USING PIXEL ELECTRODE (ITO) AS MATERIAL WITH HIGH









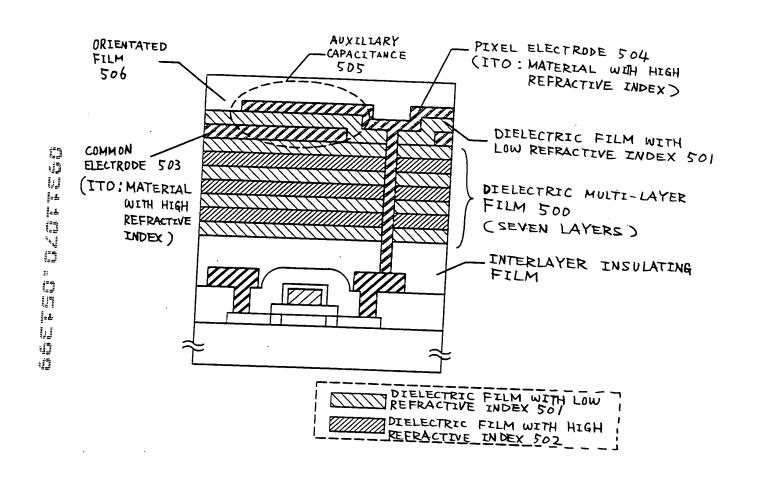
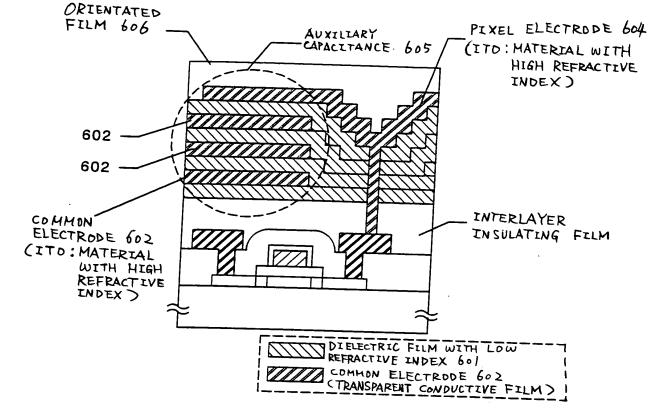


Fig. 5



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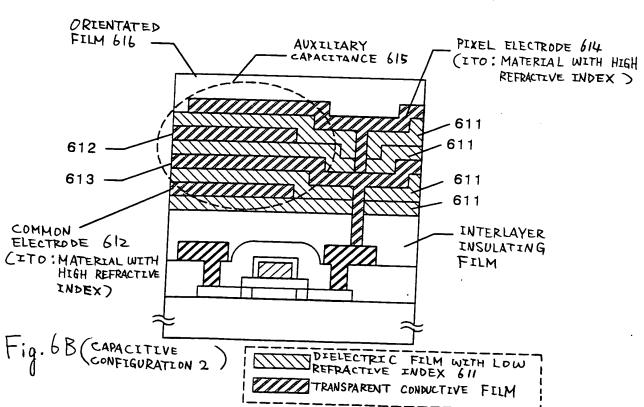
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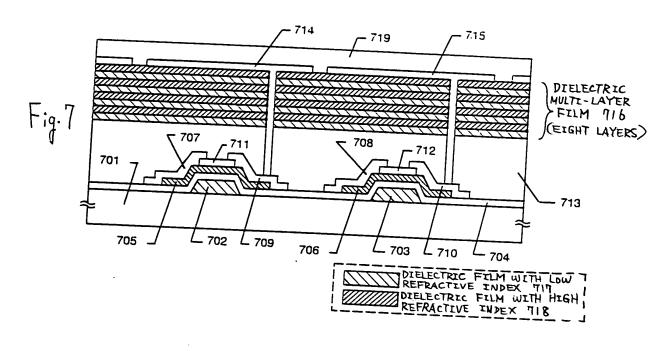
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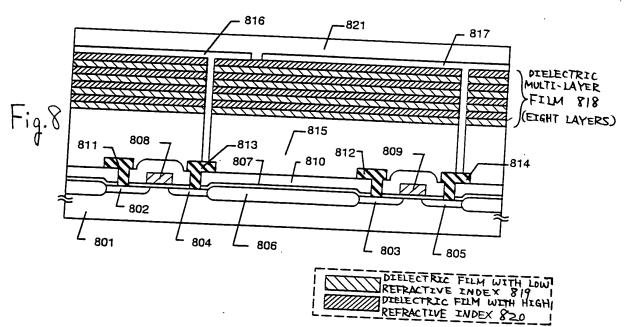
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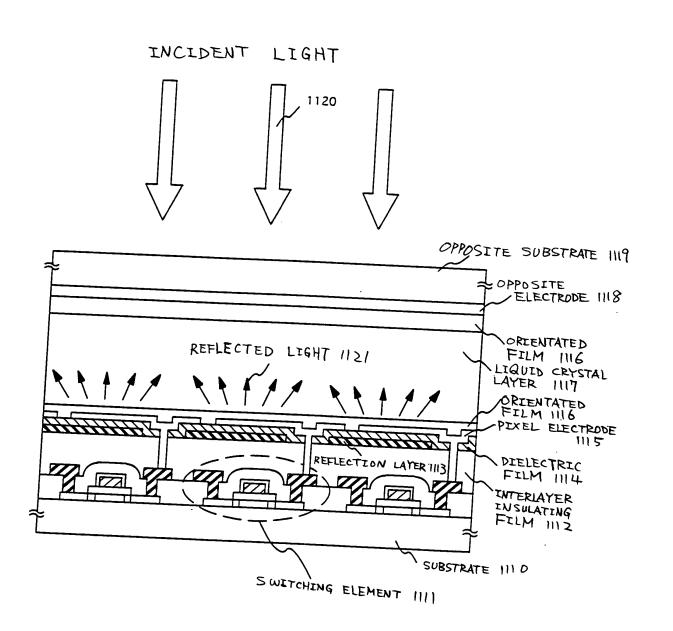
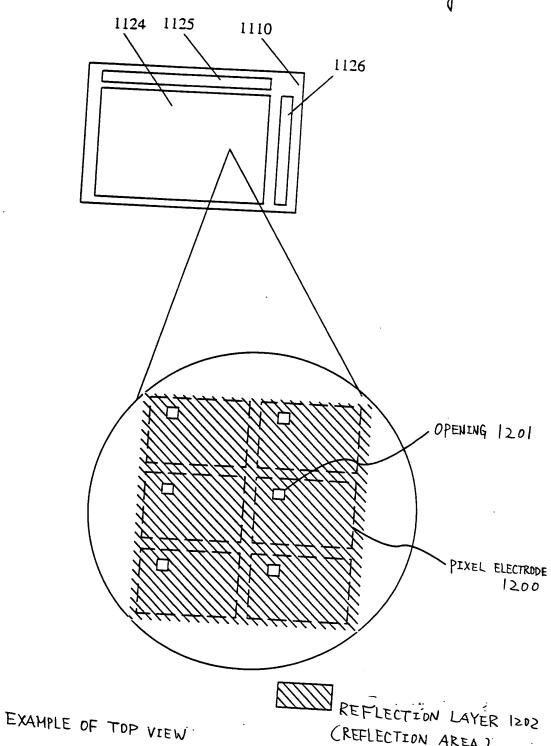
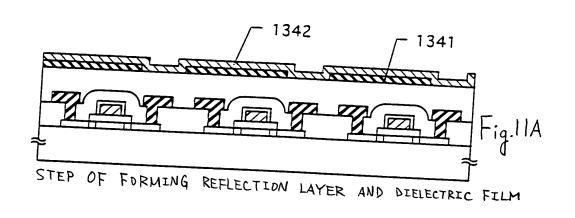


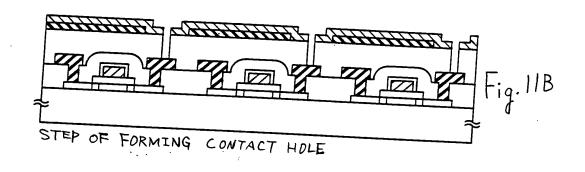
Fig. 9

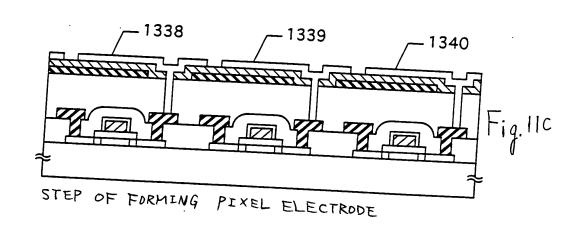
Fig. 10



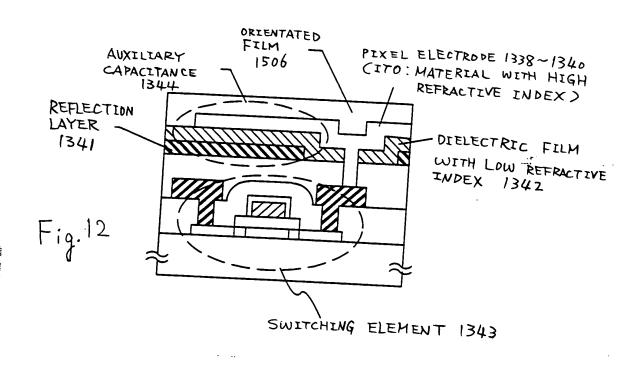
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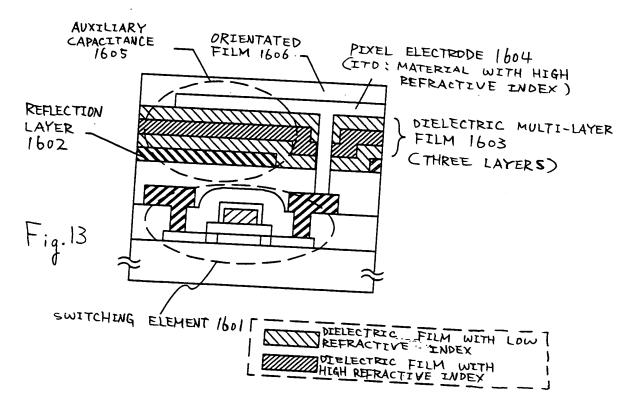












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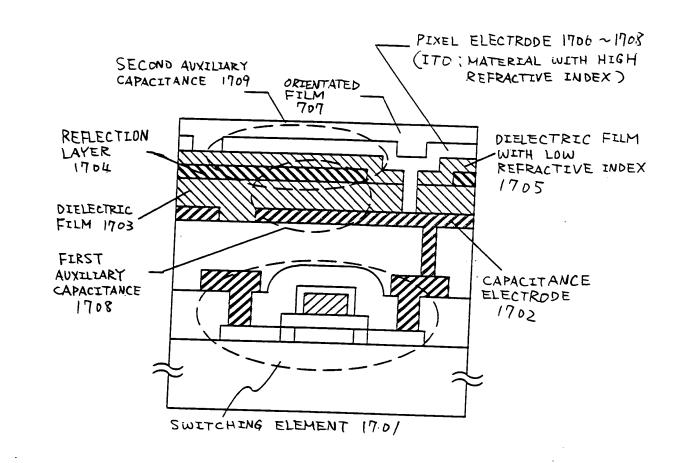
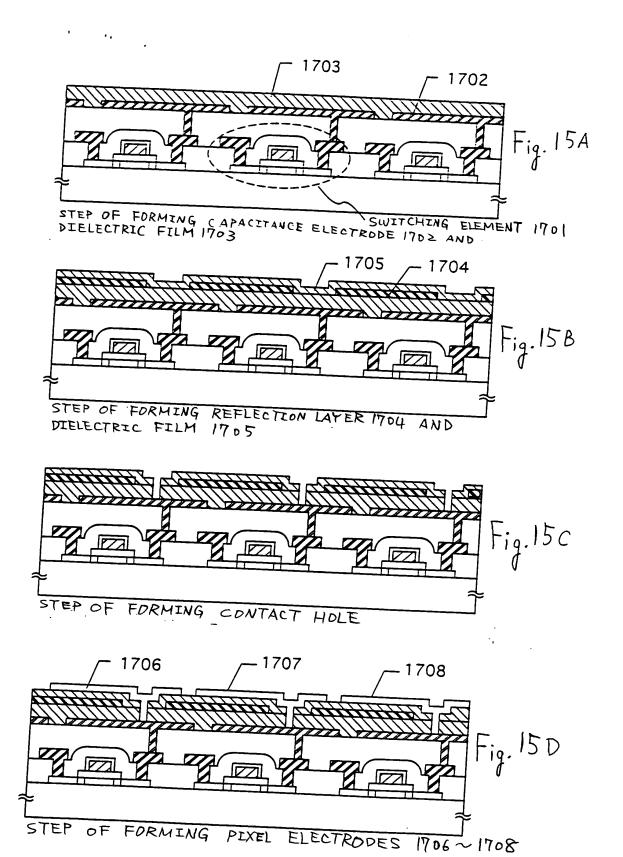
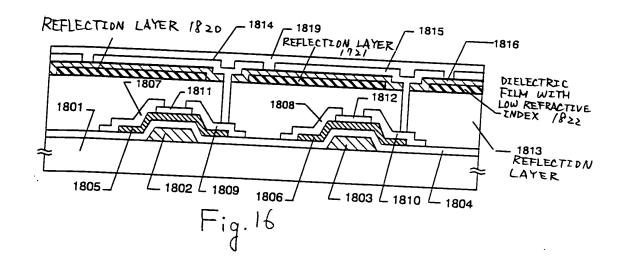
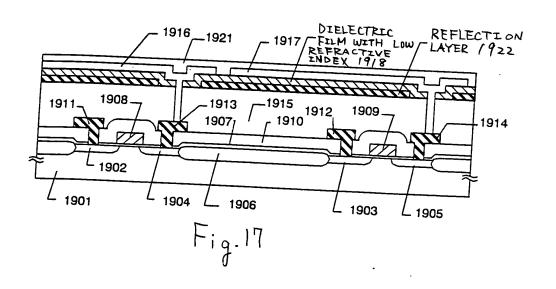
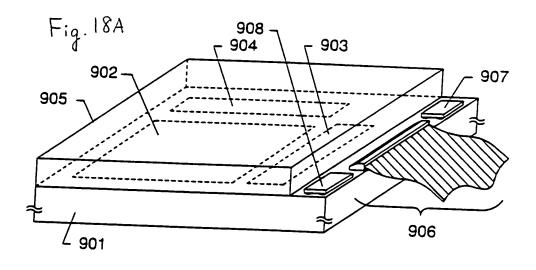


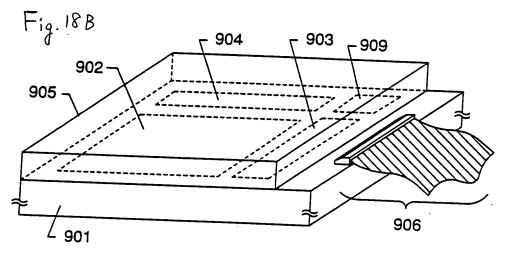
Fig. 14









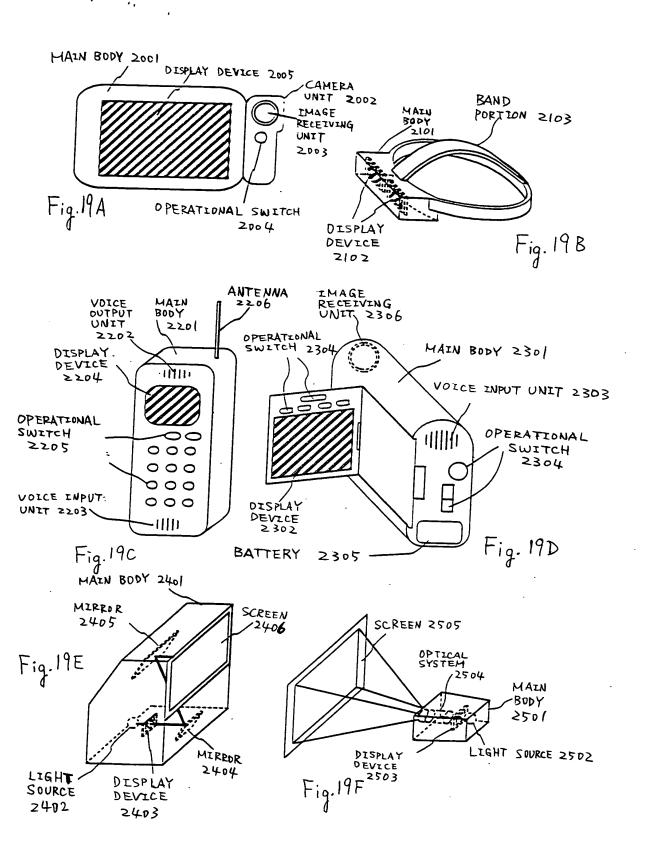


901: ACTIVE MATRIX SUBSTRATE 902: PIXEL MATRIX CIRCUIT

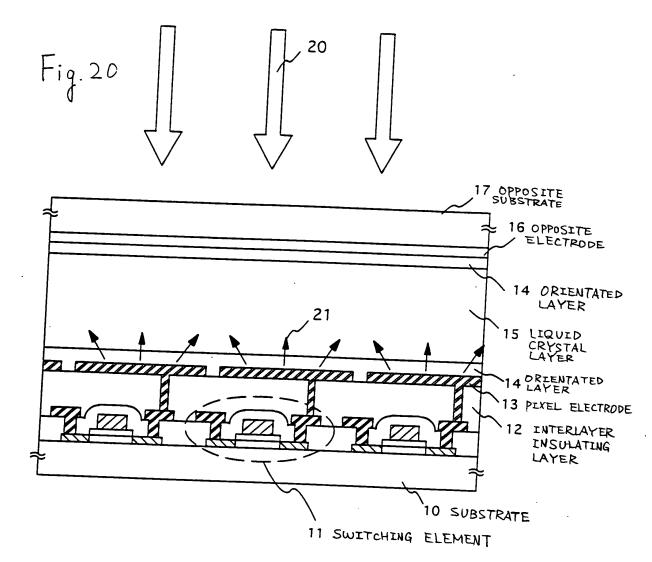
903 : SOURCE-SIDE DRIVER CIRCUIT 904: GATE-SIDE DRIVER CIRCUIT 905 : DPPOSING SUBSTRATE 9.4. ED.

906: FPC

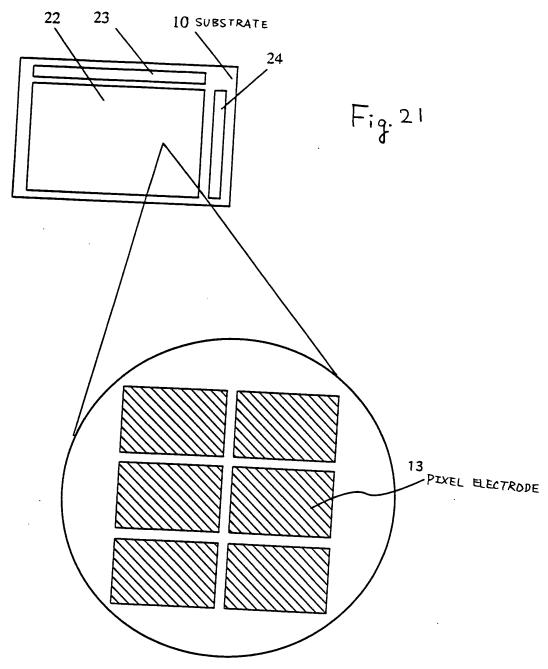
909: LOGIC CIRCUIT







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EXAMPLE OF TOP VIEW

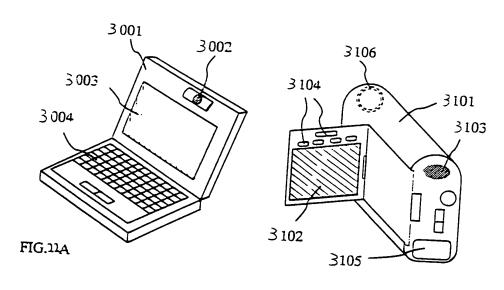
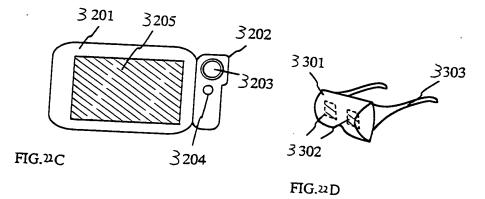
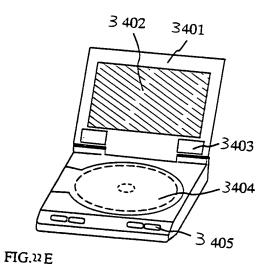


FIG.22B





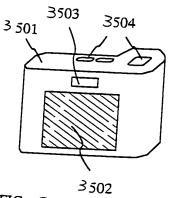


FIG.22F

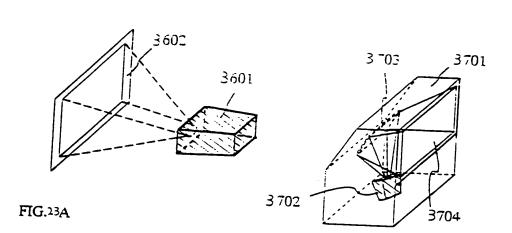


FIG.23B

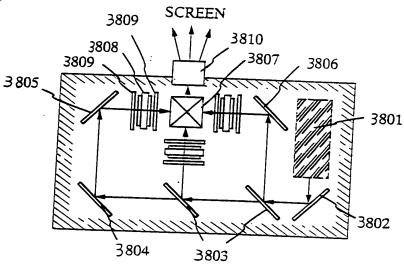
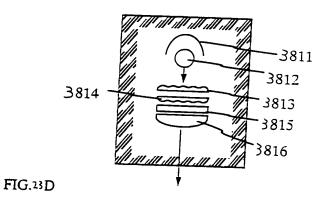


FIG.23C



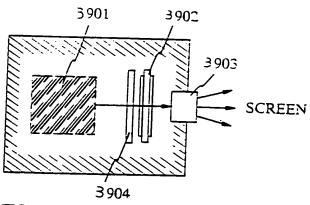


FIG.24A

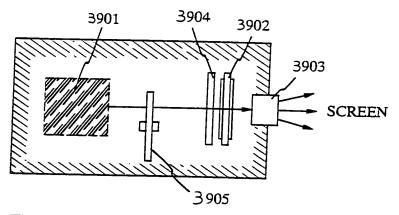


FIG.24B

